HOLT INTEGRATED CIRCUITS INC.

HI-35880

ARINC 429 Receiver with SPI Interface

March 2021

GENERAL DESCRIPTION

The HI-35880 from Holt Integrated Circuits is a silicon gate CMOS device for interfacing a Serial Peripheral Interface (SPI) enabled microcontroller to an ARINC 429 serial bus. It is a drop-in replacement for Holt's popular HI-3588, with a much improved SPI of 12 MHz. This greatly improves host efficiency over the previous device.

The HI-35880 provides one receiver with user-programmable label recognition for any combination of 256 possible labels, a 32 by 32 Receive FIFO and an analog line receiver. Receive FIFO status can be monitored using the programmable external interrupt pin, or by polling the HI-35880 Status Register. Other features include the ability to switch the bit-significance of ARINC 429 labels. The ARINC input pins are available with different input resistance values to provide flexibility when adding external lightning protection circuitry.

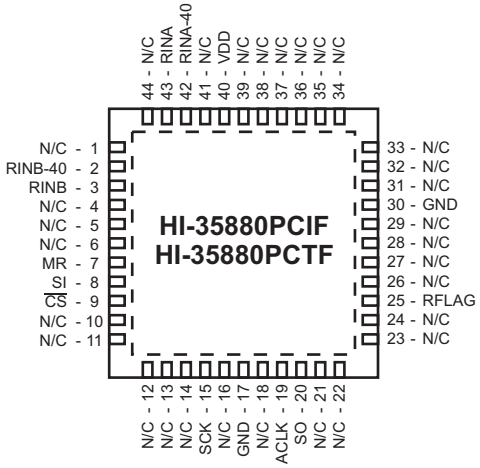
The Serial Peripheral Interface minimizes the number of host interface signals allowing for a small footprint device which can be interfaced to a wide variety of industry-standard microcontrollers supporting SPI. Alternatively, the SPI signals may be controlled using just four general purpose I/O port pins from a microcontroller or custom FPGA. The SPI and all control signals are CMOS and TTL compatible and support 3.3V or 5V operation.

The HI-35880 checks received data against ARINC 429 electrical, timing and protocol requirements. ARINC 429 databus timing comes from a 1 MHz clock input, or an internal counter can derive it from higher clock frequencies having certain fixed values, possibly the external host processor clock.

FEATURES

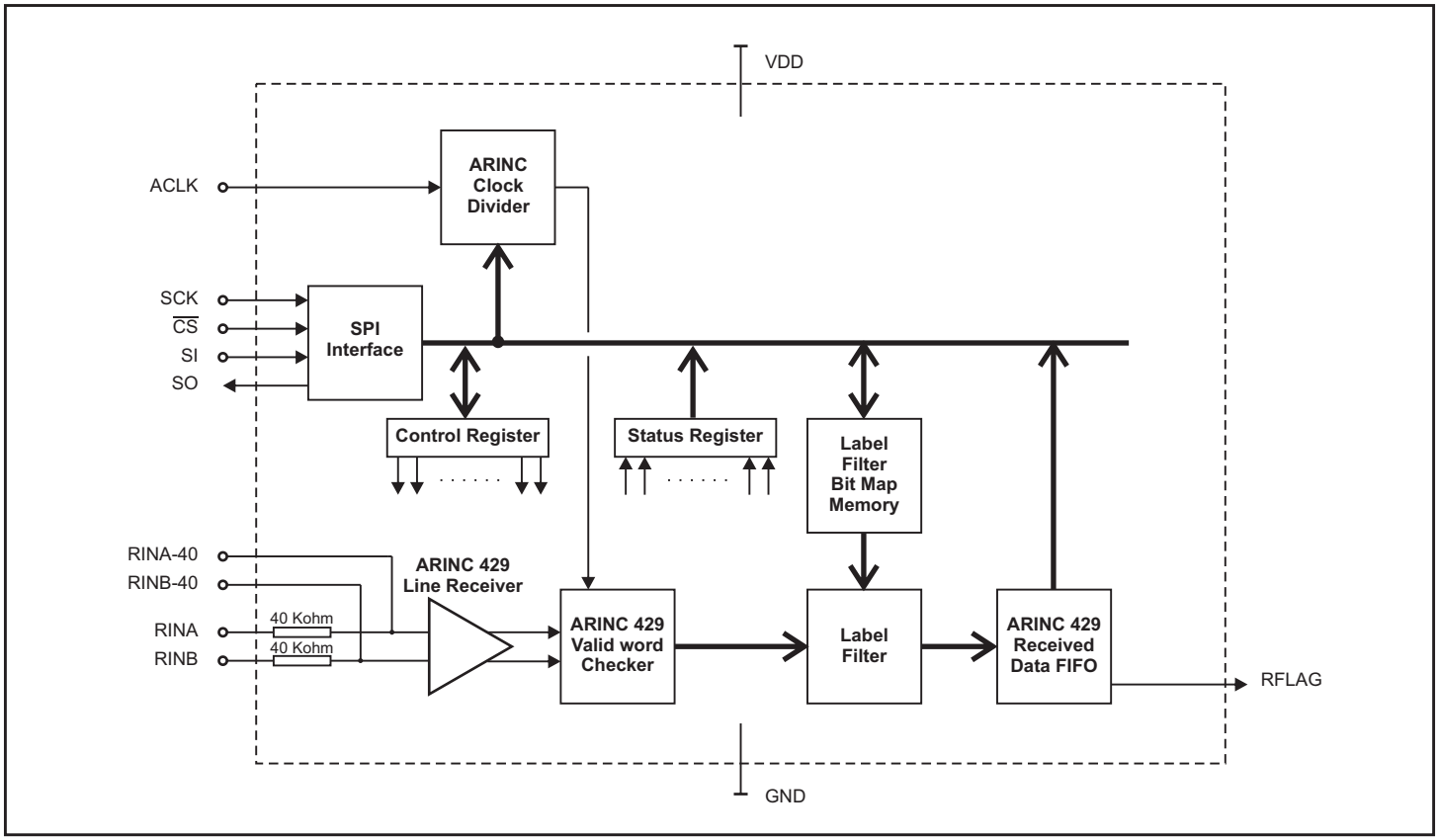
- ARINC specification 429 compliant
- 3.3V or 5.0V logic supply operation
- Drop-in replacement for Holt's HI-3588 with improved SPI host interface (12 MHz)
- On-chip analog line receiver connects directly to ARINC 429 bus
- Programmable label recognition for 256 labels
- 32 x 32 Receive Data FIFO
- Programmable data rate selection
- High-speed, four-wire, 12 MHz SPI
- Label bit-order control
- Parity checking may be disabled to allow 32-bit data reception
- Low power
- Industrial & extended temperature ranges

PIN CONFIGURATIONS (Top View)



44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)

BLOCK DIAGRAM



PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION	INTERNAL PULL UP / DOWN
RINB	INPUT	ARINC receiver negative input. Direct connection to ARINC 429 bus	
RINB-40	INPUT	Alternate ARINC receiver negative input. Requires external 40K ohm resistor	
MR	INPUT	Master Reset. A positive pulse clears the Receiver data FIFO and flags	10K ohm pull-down
SI	INPUT	SPI interface serial data input	10K ohm pull-down
$\overline{CS}$	INPUT	Chip select. Data is shifted into SI and out of SO when $\overline{CS}$ is low.	10K ohm pull-up
SCK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK	10K ohm pull-down
GND	POWER	Chip 0V supply. Note BOTH GND pins MUST be connected	
ACLK	INPUT	Master timing source for the ARINC 429 receiver	10K ohm pull-down
SO	OUTPUT	SPI interface serial data output	
RFLAG	OUTPUT	Goes high when ARINC 429 receiver FIFO is empty (CR15=0), or full (CR15=1)	
VDD	POWER	3.3V or 5.0V logic power	
RINA-40	INPUT	Alternate ARINC receiver positive input. Requires external 40K ohm resistor	
RINA	INPUT	ARINC receiver positive input. Direct connection to ARINC 429 bus	

INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-35880. When $\overline{CS}$ goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first positive edge. The op code is fed into the SI pin, most significant bit first.

For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written: 16-bit writes to Control Register, 32-bit ARINC word writes to transmit FIFO or 256-bit writes to the label-matching enable/disable table.

For read instructions, the most significant bit of the requested data word appears at the SO pin after the last op code bit is clocked into the decoder, at the next falling SCK edge. As in write instructions, data field bit-length varies with read instruction type.

Table 1 lists all instructions. Instructions that perform a reset or set are executed after the last SI bit is received while $\overline{CS}$ is still low.

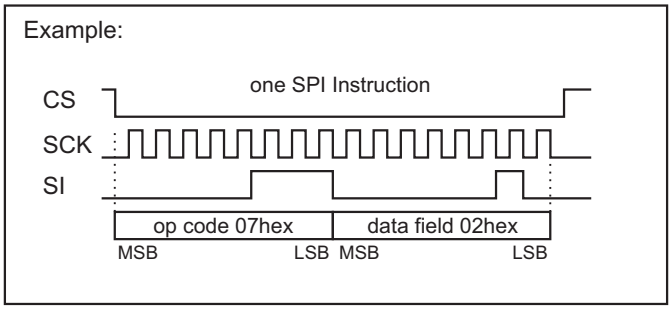


TABLE 1. DEFINED INSTRUCTION OP CODES

OP CODE Hex	DATA FIELD	DESCRIPTION
00	None	No instruction implemented
01	None	After the 8th op-code bit is received, perform Master Reset (MR)
02	None	After the 8th op-code bit is received, reset all label selections
03	None	After the 8th op-code bit is received, set all the label selections
04	8 bits	Reset label at address specified in data field
05	8 bits	Set label at address specified in data field
06	256 bits	Starting with label FF hex, consecutively set or reset each label in descending order For example, a Data Field pattern starting with 1011 will set labels FF, FD, and FC hex and reset label FE hex.
07	8 bits	Programs a division of the ACLK input. If the divided ACLK frequency is 1 MHz and Control Register bit CR1 is set, the ARINC receiver operates from the divided ACLK clock. Allowable values for division rate are X1, X2, X4, X8, or XA hex. Any other programmed value results in no clock. Note: ACLK input frequency and division ratio must result in 1 MHz clock.
08	32 bits	Read the next word in the Receive FIFO. If the FIFO is empty, it will read zeros
09	None	This instruction is reserved for factory test only
0A	8 bits	Read the Status Register
0B	16 bits	Read the Control Register
0C	8 bits	Read the ACLK divide value programmed previously using op code 07 hex
0D	256 bits	Read the Label look-up memory table consecutively starting with address FF hex
0E	None	No instruction implemented
0F	None	No instruction implemented
10	16 bits	Write the Control Register

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

The HI-35880 contains a 16-bit Control Register which is used to configure the device. Control Register bits CR15 - CR0 are loaded from a 16-bit data value appended to SPI instruction 10 hex. The Control Register contents may be read using SPI instruction 0B hex. Each bit of the Control Register has the following function:

CR Bit	FUNCTION	STATE	DESCRIPTION
CR0 (LSB)	Receiver Data Rate Select	0	Data rate = CLK/10 (ARINC 429 High-Speed)
		1	Data rate = CLK/80 (ARINC 429 Low-Speed)
CR1	ARINC Clock Source Select	0	ARINC CLK = ACLK input frequency
		1	ARINC CLK = ACLK divided by the value programmed with SPI Instruction 07 hex
CR2	Enable Label Recognition	0	Label recognition disabled
		1	Label recognition enabled
CR3	-	X	Not used
CR4	Receiver Parity Check Enable	0	Receiver parity check disabled
		1	Receiver odd parity check enabled
CR5	Receiver Enable	0	Disable receiver. The HI-35880 ignores all ARINC 429 data bus traffic
		1	Normal operation
CR6	Receiver Decoder	0	Receiver decoder disabled
		1	ARINC bits 10 and 9 must match CR7 and CR8
CR7	-	-	If receiver decoder is enabled, the ARINC bit 10 must match this bit
CR8	-	-	If receiver decoder is enabled, the ARINC bit 9 must match this bit
CR9	-	X	Not used
CR10	-	X	Not used
CR11	ARINC Label Bit Order	0	Label bit order reversed (SeeTable 2)
		1	Label bit order same as received (See Table 2)
CR12	-	X	Not used
CR13	-	X	Not used
CR14	-	X	Not used
CR15 (MSB)	RFLAG Definition	0	FLAG goes high when receive FIFO is empty
		1	RFLAG goes high when receive FIFO is full

STATUS REGISTER

The HI-35880 contains an 8-bit Status Register which can be interrogated to determine status of the ARINC Receive FIFO. The Status Register is read using SPI instruction 0A hex. Unused bits are undefined and may be read as either “1” or “0”. The following table defines the Status Register bits.

SR Bit	FUNCTION	STATE	DESCRIPTION
SR0 (LSB)	Receive FIFO Empty	0	Receiver FIFO contains valid data Sets to One when all data has been read. RFLAG pin reflects the state of this bit when CR15=”0”
		1	Receiver FIFO is empty
SR1	Receive FIFO Half Full	0	Receiver FIFO holds less than 16 words
		1	Receiver FIFO holds at least 16 words
SR2	Receive FIFO Full	0	Receiver FIFO not full. RFLAG pin reflects the state of this bit when CR15=”1”
		1	Receiver FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period
SR3	Not used	X	Undefined
SR4	Not used	X	Undefined
SR5	Not used	X	Undefined
SR6	Not used	0	Always “0”
SR7 (MSB)	Not used	0	Always “0”

ARINC 429 DATA FORMAT

Control Register bit CR11 controls how individual bits in the received ARINC word are mapped to the HI-35880 SPI data word bits during data read or write operations. The following table describes this mapping:

Table 2. SPI / ARINC bit-mapping

SPI Order	1	2 - 22	23	24	25	26	27	28	29	30	31	32
ARINC bit	32	31 - 11	10	9	1	2	3	4	5	6	7	8
CR11=0	Parity	Data	SDI	SDI	Label (MSB)	Label	Label	Label	Label	Label	Label	Label (LSB)
ARINC bit	32	31 - 11	10	9	8	7	6	5	4	3	2	1
CR11=1	Parity	Data	SDI	SDI	Label (LSB)	Label	Label	Label	Label	Label	Label	Label (MSB)

FUNCTIONAL DESCRIPTION (cont.)

ARINC 429 RECEIVER

ARINC BUS INTERFACE

Figure 1 shows the input circuit for the ARINC 429 line receiver. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

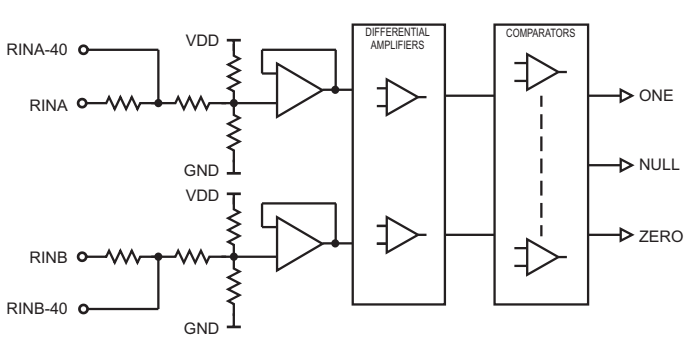


FIGURE 1. ARINC RECEIVER INPUT

The HI-35880 guarantees recognition of these levels with a common mode voltage with respect to GND less than ±30V for the worst case condition (3.15V supply and 13V signal level). Design tolerances guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal (including nulls) is outside the differential voltage ranges, the HI-35880 receiver rejects the data.

RECEIVER LOGIC OPERATION

Figure 2 is a block diagram showing receiver logic.

BIT TIMING

The ARINC 429 specification defines the following timing tolerances for received data:

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE WIDTH	5 µsec ± 5%	34.5 to 41.7 µsec

The HI-35880 accepts signals within these tolerances and rejects signals outside these tolerances. Receiver logic achieves this as described below:

1. An accurate 1MHz clock source is required to validate the receive signal timing. Less than 1% error is recommended.

2. The receiver uses three separate 10-bit sampling shift registers for Ones detection, Zeros detection and Null detection. When the input signal is within the differential voltage range for any shift register's state (One Zero or Null) sampling clocks a high bit into that register. When the receive signal is outside the differential voltage range defined for any shift register, a low bit is clocked. Only one shift register can clock a high bit for any given sample. All three registers clock low bits if the differential input voltage is between defined state voltage bands.

Valid data bits require at least three consecutive One or Zero samples (three high bits) in the upper half of the Ones or Zeros sampling shift register, and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register within the data bit interval.

A word gap Null requires at least three consecutive Null samples (three high bits) in the upper half of the Null sampling shift register and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register. This guarantees the minimum pulse width.

3. To validate the receive data bit rate, each bit must follow its preceding bit by not less than 8 samples and not more than 12 samples. With exactly 1MHz input clock frequency, the acceptable data bit rates are:

	HIGH SPEED	LOW SPEED
DATA BIT RATE MIN	83K BPS	10.4K BPS
DATA BIT RATE MAX	125K BPS	15.6K BPS

4. Following the last data bit of a valid reception, the Word Gap timer samples the Null shift register every 10 input clocks (every 80 clocks for low speed). If a Null is present, the Word Gap counter is incremented. A Word Gap count of 3 enables the next reception.

FUNCTIONAL DESCRIPTION (cont.)

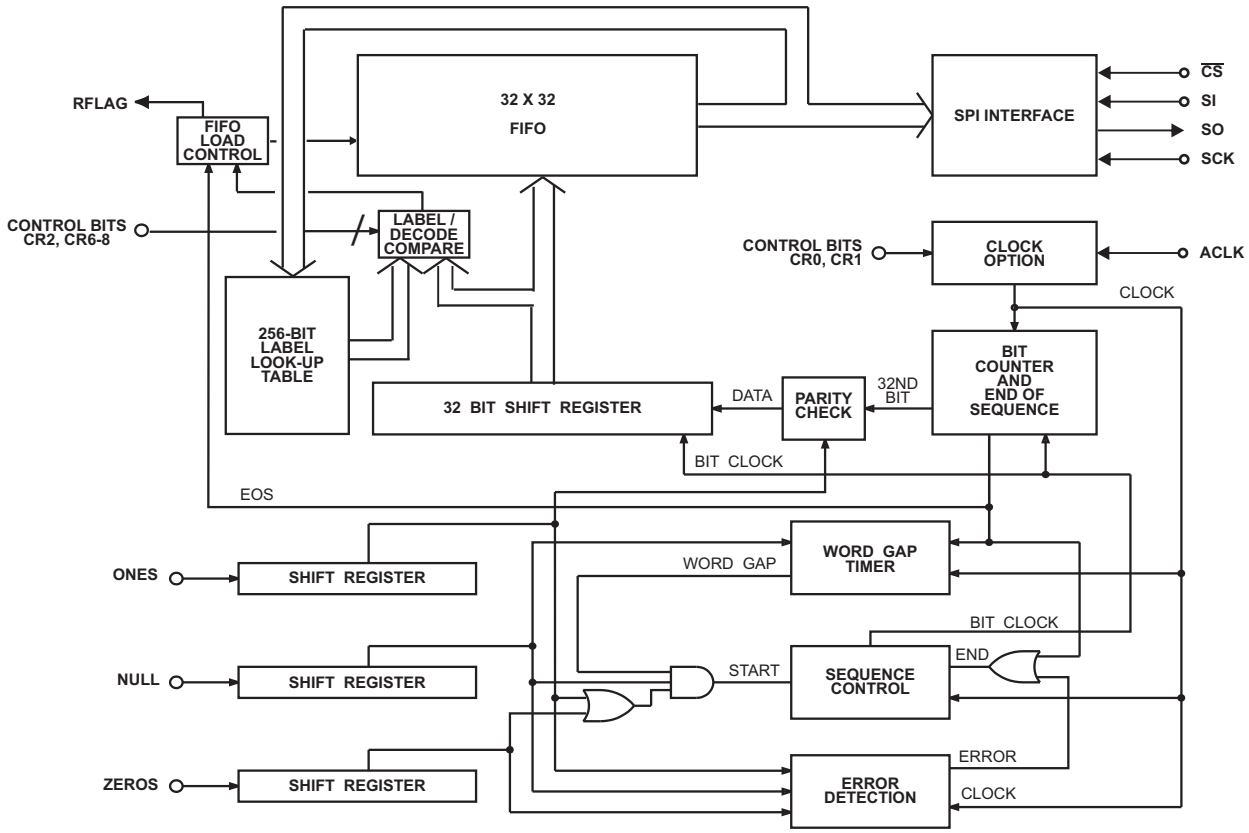


FIGURE 2. **RECEIVER BLOCK DIAGRAM**

RECEIVER PARITY

The Receiver Parity Check Enable bit (Control Register bit 4, CR4) controls how the 32nd bit of the received ARINC word is interpreted by the HI-3585 receiver.

When CR4 is set to a "0", the 32nd bit is treated as data and transferred as received from the ARINC bus to the receive FIFO.

When CR4 is set to a "1", the 32nd bit is treated as a parity error bit.

Odd Parity Received
The receiver expects the 32nd bit of the received word to indicate odd parity. If this is the case, the parity bit is reset to indicate correct parity was received and resulting word is written to the receive FIFO.

Even Parity Received
If the received word is even parity, the receiver sets the 32nd bit to a "1", indicating a parity error. The resulting word is then written to the receive FIFO.

Therefore, when CR4 is set to "1", the 32nd bit retrieved from the receiver FIFO will always be "0" when valid (odd parity) ARINC 429 words are received.

CR4	ARINC BUS 32nd bit	FIFO 32nd bit
0	data	data
1	parity bit	Error Bit: 0 = odd parity 1= odd parity error (even parity)

FUNCTIONAL DESCRIPTION (cont.)

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). Depending on the state of Control Register bits CR2, and CR6 through CR8, the received 32-bit ARINC word is then checked for correct decoding and label match before it is loaded into the 32 x 32 Receive FIFO. ARINC words that do not match required 9th and 10th ARINC bit and do not have a label match are ignored and are not loaded into the Receive FIFO. The table below describes this operation.

Once a valid ARINC word is loaded into the FIFO, the EOS signal clocks the Data Ready flip-flop to a "1" and Status Register bit 0 (SR0) to a “0”. The SR0 bit remains low until the Receive FIFO is empty. Each received ARINC word is retrieved via the SPI interface using SPI instruction 08 hex to read a single word.

Up to 32 ARINC words may be held in the Receive FIFO. Status register bit 2 (SR2) goes high when the Receive FIFO is full. Failure to unload the Receive FIFO when full causes additional received valid ARINC words to be dropped.

A FIFO half-full flag (SR1) is high when the Receive FIFO contains 16 or more ARINC words. SR1 may be interrogated by the system’s external microprocessor, allowing a 16 word data retrieval routine to be performed.

CR2	ARINC word matches Enabled label	CR6	ARINC word bits 10, 9 match CR7,8	FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore data
1	No	1	Yes	Ignore data
1	No	1	No	Ignore data
1	Yes	1	Yes	Load FIFO

LABEL RECOGNITION

The user loads the 256-bit label look-up table to specify which 8-bit incoming ARINC labels are captured by the receiver, and which are discarded. Setting a “1” in the look-up table enables processing of received ARINC words containing the corresponding label. A “0” in the look-up table causes discard of received ARINC words containing the label. The 256-bit look-up table is loaded using SPI op codes 02 hex, 03 hex or 06 hex, as described in Table 1. After the look-up table is initialized, set Control Register bit CR2 to enable label recognition.

If label recognition is enabled, the receiver compares the label in each new ARINC word against the stored look-up table. If a label match is found, the received word is processed. If no match occurs, the new ARINC word is discarded and no indicators of received ARINC data are presented.

READING THE LABEL LOOK-UP TABLE

The contents of the Label Look-up table may be read via the SPI interface using instruction 0D hex as described in Table 1.

LINE RECEIVER INPUT PINS

The HI-35880 has two sets of Line Receiver input pins, RINA/B and RINA/B-40. Only one pair may be used to connect to the ARINC 429 bus. The unused pair must be left floating. The RINA/B pins may be connected directly to the ARINC 429 bus. The RINA/B-40 pins require external 40K ohm resistors in series with each ARINC input. These do not affect the ARINC receiver thresholds. By keeping excessive voltage outside the device, this option is helpful in applications where lightning protection is required.

When using the RINA/B-40 pins, each side of the ARINC bus must be connected through a 40K ohm series resistor in order for the chip to detect the correct ARINC levels. The typical 10 Volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 40K ohm resistors, they are just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

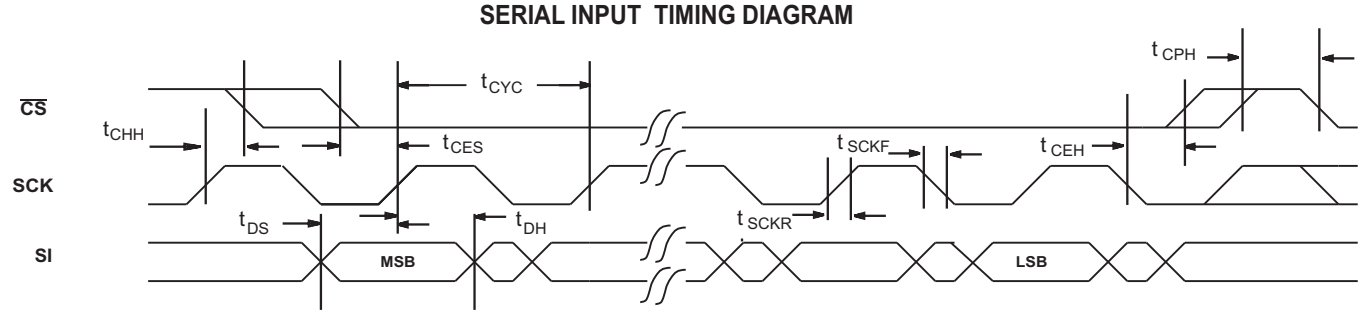
Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

MASTER RESET (MR)

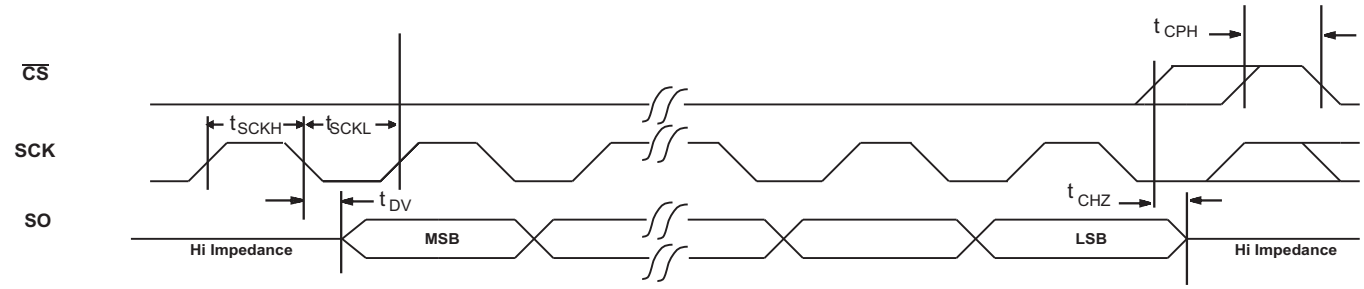
Assertion of Master Reset causes immediate termination of data reception. The receive FIFO, Status Register FIFO flags and the FIFO status RFLAG pin is also cleared. The Control Register is not affected by Master Reset.

TIMING DIAGRAMS

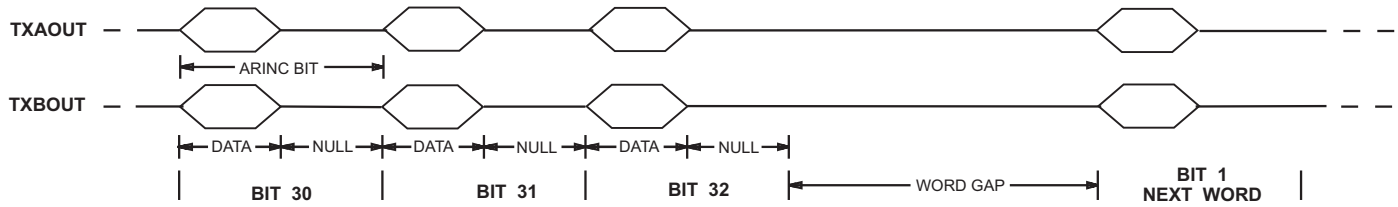
SERIAL INPUT TIMING DIAGRAM



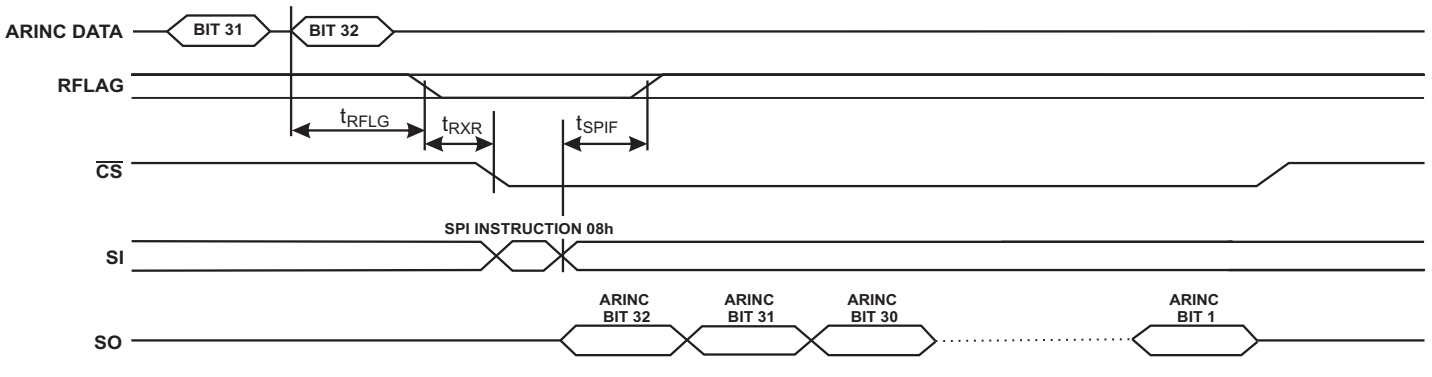
SERIAL OUTPUT TIMING DIAGRAM



DATA RATE - EXAMPLE PATTERN



RECEIVER OPERATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltages V_{DD} ..... -0.3V to +7.0V	Power Dissipation at 25°C Plastic Quad Flat Pack .....1.5 W, derate 10mW/°C
Voltage at pins RINA, RINB ..... -120V to +120V	DC Current Drain per pin ..... ±10mA
Voltage at any other pin ..... -0.3V to V_{DD} +0.3V	Storage Temperature Range ..... -65°C to +150°C
Solder temperature (Leads) ..... 280°C for 10 seconds (Package) ..... 260°C	Operating Temperature Range (Industrial): .... -40°C to +85°C (Hi-Temp): .....-55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V or 5.0V , GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

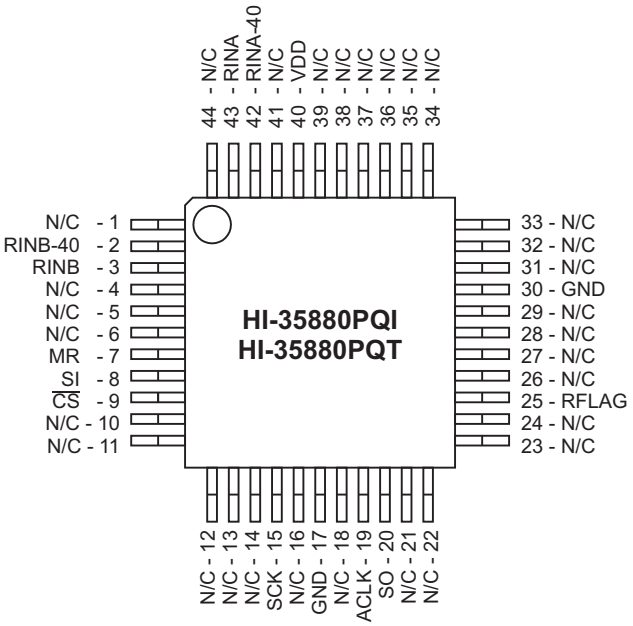
PARAMETER		SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
ARINC INPUTS - Pins RINA, RINB, RINA-40 (with external 40KOhms), RINB-40 (with external 40KOhms)							
Differential Input Voltage: (RINA to RINB)	ONE ZERO NULL	V_{IH} V_{IL} V_{NUL}	Common mode voltages less than ±30V with respect to GND	6.5 -13.0 -2.5	10.0 -10.0 0	13.0 -6.5 2.5	V V V
Input Resistance:	Differential To GND To V_{DD}	R_I R_G R_H		- - -	140 140 100	- - -	KΩ KΩ KΩ
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -450		200	µA µA
Input Capacitance: (Guaranteed but not tested)	Differential To GND To V_{DD}	C_I C_G C_H	(RINA to RINB)			20 20 20	pF pF pF
LOGIC INPUTS							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		80% VDD		 20% VDD	V V
Input Current:	Input Sink Input Source Pull-down Current (MR, SI, SCK, ACLK pins) Pull-up Current ($\overline{CS}$ Pin)	I_{IH} I_{IL} I_{PD} I_{PU}		 -1.5 -100		1.5 100 	µA µA µA µA
LOGIC OUTPUTS							
Output Voltage:	Logic "1" Output Voltage Logic "0" Output Voltage	V_{OH} V_{OL}	I_{OH} = -100µA I_{OL} = 1.0mA	90%VDD		 10% VDD	V V
Output Current: (All Outputs & Bi-directional Pins)	Output Sink Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{DD} - 0.4V	1.6		 -1.0	mA mA
Output Capacitance:		C_O			15		pF
Operating Voltage Range							
		VDD		3.15		5.25	V
Operating Supply Current							
VDD		I_{DD}			2.5	7	mA

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3V or 5.0V, GND = 0V, TA = Operating Temperature Range and fclk=1MHz ±0.1% with 60/40 duty cycle

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
SPI INTERFACE TIMING					
SCK clock period	t_{CYC}	80			ns
$\overline{CS}$ active after last SCK rising edge	t_{CHH}	10			ns
$\overline{CS}$ setup time to first SCK rising edge	t_{CES}	10			ns
$\overline{CS}$ hold time after last SCK falling edge	t_{CEH}	20			ns
$\overline{CS}$ inactive between SPI instructions	t_{CPH}	20			ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10			ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10			ns
SCK rise time	t_{SCKR}			5	ns
SCK fall ime	t_{SCKF}			5	ns
SO valid after SCK falling edge	t_{DV}			20	ns
SO high-impedance after $\overline{CS}$ inactive	t_{CHZ}			50	ns
Master Reset pulse width	t_{MR}	100			ns
RECEIVER TIMING					
Delay - Last bit of received ARINC word to RFLAG(Full or Empty) - Hi Speed	t_{RFLG}			16	µs
Delay - Last bit of received ARINC word to RFLAG(Full or Empty) - Lo Speed	t_{RFLG}			126	µs
Received data available to SPI interface. RFLAG to $\overline{CS}$ active	t_{RXR}	0			ns
SPI receiver read or clear FIFO instruction to RFLAG	t_{SPIF}			155	ns

ADDITIONAL PIN CONFIGURATIONS (Top View)



44 - Pin Plastic Quad Flat Pack (PQFP)

ORDERING INFORMATION

HI - 35880 PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
PQ	44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PMQS)

HI - 35880 PC x F

PART NUMBER	LEAD FINISH
F	NiPdAu (Pb-free, RoHS compliant)*

*Note: NiPdAu lead finish is forward and backward compatible with both SnPb and Pb-free reflow profiles

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
PC	44 PIN PLASTIC CHIP-SCALE, QFN (44PCS)

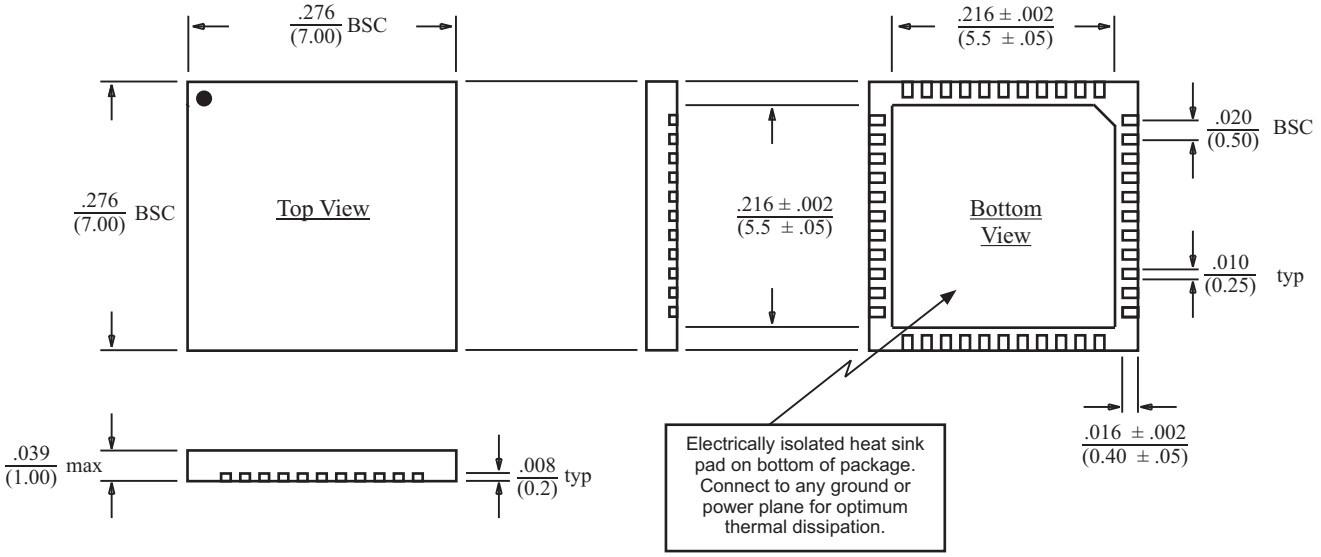
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS35880	New	12/11/2020	Initial Release
	A	03/31/2021	Change SPI Op Code 0x09 description to “reserved for factory test only”. In section “Receiving Data”, clarify that messages received to a full FIFO will be dropped.

44-PIN PLASTIC CHIP-SCALE PACKAGE

inches (millimeters)

Package Type: 44PCS

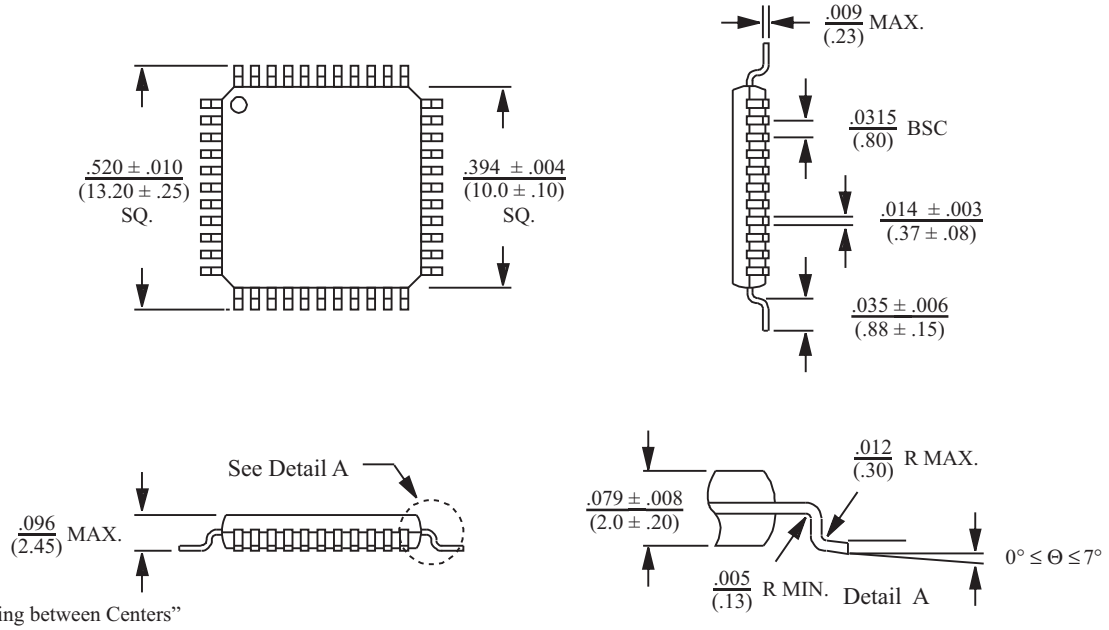


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 44PMQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)